AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A computer system, comprising:

system memory;

a voltage regulator configured to provide a supply voltage to a plurality of components in the computer system, wherein one of the components is a switching regulator;

the switching regulator, wherein the switching regulator is configured to regulate the supply voltage and to provide a termination voltage, separate from the supply voltage, to the system memory; and

a clamping circuit, wherein the clamping circuit comprises a detecting stage and a clamping stage, wherein the detecting stage is configured to activate the clamping stage when the supply voltage exceeds a first voltage level, and wherein the clamping stage is coupled to the detecting stage and configured to reduce the supply voltage in response to being activated by the detecting stage.

2. (Original) The computer system of claim 1, wherein the system memory comprises DDR SDRAM.

3. (Original) The computer system of claim 1, wherein the detecting stage comprises a voltage divider coupled to the supply voltage and configured to monitor the supply voltage, wherein the voltage divider provides a voltage activating the clamping stage when the supply voltage exceeds the first voltage level.

4. (Original) The computer system of claim 1, wherein the clamping stage is configured to reduce the supply voltage by shunting current to ground.

5. (Original) The computer system of claim 4, wherein the clamping stage comprises a shunt regulator.

6. (Original) The computer system of claim 5, wherein the clamping stage further comprises a transistor, wherein the shunt regulator is configured to provide a base current to the transistor, and wherein the transistor is configured to reduce the supply voltage by shunting current to ground when provided with the base current.

7. (Original) The computer system of claim 1, wherein the first voltage level is lower than a maximum voltage level.

8. (Original) The computer system of claim 7, wherein the clamping stage is further configured to prevent the supply voltage from exceeding the maximum voltage level.

9. (Original) The computer system of claim 7, wherein the maximum voltage level is a voltage level that causes erroneous behavior in a first portion of the components provided with the supply voltage.

10. (Original) The computer system of claim 1, wherein the detecting stage is further configured to not activate the clamping stage when the supply voltage does not exceed the first voltage level.

11. (Original) The computer system of claim 1, wherein the clamping stage is further configured to stop reducing the supply voltage when the detecting stage stops detecting that the supply voltage exceeds the first voltage level.

12. (Currently amended) A method of operating a computer system, comprising:

providing a voltage rail to a plurality of components in the computer system, wherein the voltage rail is provided by a linear regulator, and wherein the plurality of components comprise a switching regulator;

providing a termination voltage, separate from the supply voltage, to system memory, wherein the termination voltage is provided by the switching regulator;

detecting when the voltage rail exceeds a first voltage level; and

clamping the voltage rail in response to said detecting so that the voltage rail does not exceed a maximum voltage level, wherein the maximum voltage level is a voltage level that causes erroneous behavior in a first portion of the components provided with the voltage rail.

13. (Original) The method of claim 12, wherein the system memory comprises DDR SDRAM.

14. (Original) The method of claim 12, wherein said clamping only occurs while the voltage rail is detected to be exceeding the first voltage level.

15. (Original) The method of claim 12, wherein said detecting comprises using a voltage divider to measure the voltage rail.

16. (Original) The method of claim 12, wherein said clamping comprises shunting current from the voltage rail to ground.

17. (Original) The method of claim 12, wherein said clamping comprises activating a shunt regulator, wherein the shunt regulator is configured to shunt current to ground when activated.

18. (Original) The method of claim 12, wherein said clamping comprises using a shunt regulator to activate a transistor coupled to the voltage rail, wherein the transistor is configured to shunt current from the voltage rail to ground when activated.

19. (Original) The method of claim 12, wherein said clamping is done quickly enough that the voltage rail does not exceed the maximum voltage level.

20. (Original) The method of claim 19, wherein the first voltage level is lower than the maximum voltage level.

21. (Previously presented) A clamping circuit configured to clamp a voltage rail in a computer system, comprising:

a voltage divider coupled to the voltage rail and to a shunt regulator, wherein the voltage divider is configured to apply an input voltage to the shunt regulator, wherein the voltage divider is configured so that the input voltage is greater than or equal to a reference voltage level of the shunt regulator when a voltage on the voltage rail is greater than or equal to a first voltage level, and wherein the voltage divider is configured so that the input voltage is less than the reference voltage level when the voltage on the voltage rail is less than the first voltage level;

the shunt regulator coupled to the voltage divider, wherein the shunt regulator is configured to turn on when the input voltage is greater than or equal to the reference voltage level and turn off when the input voltage is less than the reference voltage level; and

a transistor coupled to the voltage rail and to the shunt regulator, wherein the transistor is configured to turn on in response to the shunt regulator turning on, wherein the transistor is configured to sink current from the voltage rail when the transistor is on to decrease the voltage on the voltage

rail below the first voltage level while the voltage rail is being supplied by a power supply, and wherein the transistor is further configured to turn off when the shunt regulator is off.

22. (Original) The clamping circuit of claim 21, further comprising a current-limiting resistor coupled between the shunt regulator and the transistor.